

Fourth International Workshop on  
**FPGAs for Software Programmers (FSP 2017)**

September 7, 2017, Ghent, Belgium  
co-located with  
International Conference on Field Programmable Logic and Applications (FPL)

## **Preface**

### **Keynote 1**

**"FPGA supported domain-specific embedded computing"**

*Dirk van den Heuvel, TOPIC Products (Not available on CD)*

### **Session 1: "High-Level Design Methodology"**

**"A Case for Better Integration of Host and Target Compilation When Using OpenCL for FPGAs"**

*Taylor Lloyd, Artem Chikin, Erick Ochoa, Karim Ali, José Nelson Amaral*

**"PCIeHLS: an OpenCL HLS framework"**

*Malte Vesper, Dirk Koch, Khoa Pham*

**"SOCAO: Source-to-Source OpenCL Compiler for Intel-Altera FPGAs"**

*Johanna Rohde, Marcos Martinez-Peiró, Rafael Gadea-Gironés*

### **Keynote 2**

**"FPGA-based Acceleration: we need source to source compilers!"**

*João M.P. Cardoso, University of Porto/FEUP/INESC-TEC (Not available on CD)*

### **Session 2: "Applications and Libraries"**

**"A Highly Efficient and Comprehensive Image Processing Library for C++-based High-Level Synthesis"**

*M. Akif Özkan, Oliver Reiche, Frank Hannig, Jürgen Teich*

**"Accelerating Linux Bash Commands on FPGAs Using Partial Reconfiguration"**

*Edson Horta, Xinzi Shen, Khoa Pham, Dirk Koch*

**"Acceleration of Solving Quadratic Assignment Problems on Programmable SoC using High Level Synthesis"**

*Kenji Kanazawa*

### **Session 3: "Analysis Tools/Short Papers"**

**"Spatial Memory Trace Prediction"**

*Nadeen Yassir Gebara, Paolo Ienne, Kermin Fleming*

**"C++ support for better hardware/software co-design in C# with SME"**

*Kenneth Skovhede, Brian Vinter*

**"On the HLS Design of Bit-Level Operations and Custom Data Types"**

*Jose Raul Garcia Ordaz, Dirk Koch*

**"Using GCC Analysis Techniques to Enable Parallel Memory Accesses in HLS"**

*Johanna Rohde, Christian Hochberger*

## **Imprint**