

Content

Keynotes

Addressing High-level Synthesis Challenges for Heterogenous Computing at the Edge..... VI
Juan Eusse, Silexica, Germany
(Not available on CD)

Architecture Virtualization as Prerequisite for Large-Scale FPGA Adoption In Software Communities VI
Christophe Bobda, University of Florida, USA
(Not available on CD)

Session 1 „HLS Acceleration and Optimization“

Accelerating Human Activity Recognition Systems on FPGAs through a DSL approach..... 1
Daniel Fernandes and João Cardoso

Accelerating Design Convergence of Automata Processing Designs with a Tiled Hierarchy 9
Tommy Tracy II, Jack Wadden, Ted Xie, Kevin Skadron and Mircea Stan

Impact of Off-Chip Memories on HLS-Generated Circuits..... 17
Abhi D. R., Ron Sass and Andrew Schmidt

Session 2 „Heterogeneous Systems and Runtime Support“

LibGalapagos: A Software Environment for Prototyping and Creating Heterogeneous FPGA and CPU Applications 27
Naif Tarafdar and Paul Chow

Run-time Performance Monitoring of Heterogenous Hw/Sw Platforms Using PAPI 34
Tiziana Fanni, Daniel Madroñal, Claudio Rubattu, Carlo Sau, Francesca Palumbo, Eduardo Juárez, Maxime Pelcat, César Sanz and Luigi Raffo

ZUCL 2.0: Virtualised Memory and Communication for ZYNQ UltraScale+ FPGAs 44
Khoa Pham, Kyriakos Paraskevas, Anuj Vaishnav, Andrew Attwood, Malte Vesper and Dirk Koch

Invited Talks and Tutorials

fpgaConvNet and f-CNNx: Towards addressing the challenges in ML application deployment VII
Christos-Savvas Bouganis, Imperial College London, UK
(Not available on CD)

OpenCL design flows for Intel and Xilinx FPGAs: Using common design patterns and dealing with vendor-specific differences	53
Tobias Kenter, Paderborn University, Germany	

Care of magical creatures – How to tame, train and feed your Alveo or Stratix FPGA card	VIII
Luciano Lavagno, Politecnico di Torino, Italy	
(<i>Not available on CD</i>)	