

Contents

Tutorials

- T1 Design Meets EDA: Gaps and Countermeasures in Analog/Mixed-Signal IC Design**
Benjamin Prautsch¹, Reimund Wittmann², Frank Schenkel³, Johannes Koelsch, Christoph Grimm⁴, Gunter Strube⁵
¹Fraunhofer IIS/EAS, Dresden, Germany; ²Imst GmbH, Kamp-Lintfort, Germany; ³Muneda GmbH, Unterhaching, Germany; ⁴TU Kaiserslautern, Kaiserslautern, Germany; ⁵Blu Business Development, Gröbenzell, Germany
- T2 Qubit Gate Quality Loss Through Circuit Parasitics and Noise 19**
Lotte Geck¹, Stefan van Waasen^{1,2}
¹Central Institute of Engineering, Electronics and Analytics, Electronic Systems, Forschungszentrum Jülich GmbH, Jülich, Germany; ²Faculty of Engineering, Communication Systems, University of Duisburg-Essen, Germany
- T3 Modeling Power Supply Noise in RF SoCs..... 24**
Jonas Meier, Florian Menke, Lantao Wang, Tim Lauber, Ralf Wunderlich and Stefan Heinen
Chair of Integrated Analog Circuits and RF Systems, RWTH Aachen University, Aachen, Germany
- T4 High-Performance Flexible and Printed Electronics Based on Inorganic Semiconducting Structures 30**
Abhishek Singh Dahiya, Dhayalan Shakthivel, Yogeenth Kumaresan and Ravinder Dahiya
Bendable Electronics and Sensing Technologies (BEST) Group, University of Glasgow, Glasgow, UK
- T5 On-Time RFIC Development with Fast EM Simulation and Integrated Design Flow**
Fadoua Gacim; Anton Klotz, Cadence Design Systems, Germany
- T6 Metastable states in ECL- and CML designs and their consideration by design of TDCs with picoseconds resolutions**
Gerald Kell, Daniel Schulz, Technische Hochschule Brandenburg; FB Informatik und Medien, Germany
- T7 Optimizing Neural Networks for Embedded Hardware 36**
Domenik Helms², Karl Amende³, Saqib Bukhari⁴, Thies de Graaff², Alexander Frickenstein¹, Frank Hafner⁴, Tobias Hirscher³, Sven Mantowsky⁴, Georg Schneider⁴, and Manoj-Rohit Vemparala¹
¹BMW AG, Munich, Germany; ²OFFIS e.V., Oldenburg, Germany; ³Valeo, Kronach, Germany; ⁴ZF Friedrichshafen AG, Saarbrücken/Friedrichshafen, Germany
- T8 The Essential Role of Procedural Approaches in Electronic Design Automation 42**
Daniel Marolt¹, Jürgen Scheible¹, Göran Jerke², Vinko Marolt²
¹Electronics & Drives, Reutlingen University Reutlingen, Germany; ²Automotive Electronics, Robert Bosch GmbH Reutlingen, Germany

SMACD 2021

A1 | Competition (1)

Chair: Engin Afacan, Gebze Technical University, Turkey

- A1.1 Trash or Treasure? Machine-learning based PCB layout anomaly detection with AnoPCB ... 48**
 Henning Franke¹, Paul Kucera¹, Julian Kuners¹, Tom Reinhold², Martin Grabmann²,
 Patrick Mäder¹, Marco Seeland² and Georg Gläser¹
¹Technische Universität Ilmenau, Germany; ²IMMS Institut für Mikroelektronik- und Mechatronik-
 Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany
- A1.2 A Deep Learning Toolbox for Analog Integrated Circuit Placement 52**
 António Gusmão^{1,2}, António Canelas¹, Nuno Horta^{1,2}, Nuno Lourenço¹ and Ricardo Martins¹
¹Instituto de Telecomunicações, Lisboa, Portugal; ²Instituto Superior Técnico – Universidade de
 Lisboa, Lisboa, Portugal
- A1.3 A Differential Evolution based Methodology for Parameter Extraction of Behavioral Models
 of Electronic Components. 56**
 Gazmend Alia^{1,2}, Andi Buzo¹, Daniel Ludwig¹, Linus Maurer² and Georg Pelz¹
¹Infineon Technologies AG, Bundeswehr University Munich, Munich, Germany;
²Bundeswehr University Munich, Munich, Germany

A2 | Machine Learning SS

Chair: Ralf Sommer, TU Ilmenau & IMMS GmbH, Germany

- A2.1 Machine Learning in the Analog Circuit Simulation Loop 60**
 Petar Tzenov and Ahmed Sokar, Infineon Technologies AG, Neubiberg, Germany
- A2.2 Bringing Structure into Analog IC Placement with Relational Graph Convolutional
 Networks. 64**
 António Gusmão^{1,2}, Nuno Horta^{1,2}, Nuno Lourenço¹ and Ricardo Martins¹
¹Instituto de Telecomunicações, Lisboa, Portugal; ²Instituto Superior Técnico – Universidade de
 Lisboa, Lisboa, Portugal
- A2.3 Machine Learning in Charge: Automated Behavioral Modeling of Charge Pump Circuits ... 68**
 Martin Grabmann¹, Christian Landrock² and Georg Gläser¹
¹IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH),
 Ilmenau, Germany; ²X-FAB Global Services GmbH, Erfurt, Germany

A3 | RF Systems (1)

Chair: Nuno Lourenço, Instituto de Telecomunicações, Portugal

- A3.1 Frequency-Limited Reduction of RLCK Circuits via Second-Order Balanced Truncation ... 72**
 Olympia Axelou, Dimitrios Garyfallou and George Floros, Department of Electrical and Computer
 Engineering, University of Thessaly, Volos, Greece
- A3.2 A Mixed Time-Frequency RF Simulation Technique Based on Numerical Time-Slot
 Partitioning 76**
 Jorge Oliveira, School of Technology and Management, Polytechnic of Leiria, Leiria, Portugal and
 Instituto de Telecomunicações, University of Aveiro, Aveiro, Portugal

- A3.3 Application of Asymmetric Crosstalk Harnessed Signaling on 3D Hexagonal Interconnect Arrays** 80
 Daniel Iparraguirre¹ and José Delgado-Frías²
¹Intel Corporation, Hillsboro, OR, USA; ²Washington State University, Pullman, WA, USA

A4 | Competition (2)

Chair: Engin Afacan, Gebze Technical University, Turkey

- A4.1 Adaptive Test Bench Generation, Simulation and Parameter Extraction for AMS Circuitry** 84
 Alexander Meyer, Leon Weihs, Ralf Wunderlich and Stefan Heinen, Integrated Analog Circuits and RF Systems Laboratory, RWTH Aachen University, Aachen, Germany
- A4.2 Monitoring Analog Circuit Performance using Adaptive Filters and RSM-based Behavioral Models** 88
 Maike Taddiken, Steffen Paul and Dagmar Peters-Drolshagen, Institute of Electrodynamics and Microelectronics (ITEM.me), University of Bremen, Germany

A5 | Device Modelling (1)

Chair: Nicola Femia, University of Salerno, Italy

- A5.1 A Compact Model for Scalable MTJ Simulation** 92
 Fernando García-Redondo¹, Pranay Prabhat¹, Mudit Bhargava² and Cyrille Dray³
¹Arm Ltd, Cambridge, UK; ²Arm Inc, Austin, USA; ³Arm Ltd, La Paros, France
- A5.2 A Quantitive Analysis of the Recovery Effect in Batteries from Datasheets** 96
 Alberto Bocca, Yukai Chen, Wenlong Wang, Alberto Macii, Enrico Macii and Massimo Poncino
 Department of Control and Computer Engineering, Politecnico di Torino, Torino, Italy

A6 | RF Systems (2)

Chair: Günhan Dündar, Bogazici University, Turkey

- A6.1 A Phase Error Correction Algorithm for RF Energy Harvesters Using Two Antennas** 100
 Ali Dogus Güngördü, Didem Erol, Alican Çağlar and Mustafa Berke Yelten
 Istanbul Technical University, Electronics and Communications Engineering, Istanbul, Turkey
- A6.2 Robust Design Methodology for RF LNA including Corner Analysis** 104
 Antonio Dionisio Martínez-Pérez¹, Francisco Aznar², Guillermo Royo¹, Pedro Martinez¹ and Santiago Celma¹
¹Group of Electronic Design (GDE), Universidad de Zaragoza, Zaragoza, Spain; ²Group of Electronic Design (GDE), Centro Universitario de la Defensa, Zaragoza, Spain
- A6.3 Event-Driven Modeling and Simulation of 5G NR-Band RF Transceiver in SystemVerilog** . . 108
 Chan Young Park and Jaeh Kim, Electrical and Computer Engineering Department, Seoul National University, Seoul, Korea

A7 | Wireless Power SS

Chair: Giulia Di Capua, University of Cassino and Southern Lazio, Italy

A7.1 Sensitivity analysis in dynamic WPT systems based on non-intrusive stochastic methods . . . 112Paul Lagouanelle^{1,3}, Giulia Di Capua⁴, Nicola Femia⁵, Fabio Freschi³, Antonio Maffucci⁴, Lionel Pichon¹ and Salvatore Ventre⁴¹Group of Electrical Eng., Paris, CNRS, CentraleSupélec, Université Paris-Saclay, Gif-sur-Yvette, France; ³Department of Energy, Politecnico of Torino, Turin, TO, Italy; ⁴Department of Electrical and Information Eng., University of Cassino and Southern Lazio, Cassino, FR, Italy; ⁵Department of Information and Electrical Eng. and Applied Math., University of Salerno, Fisciano, SA, Italy**A7.2 Performance Analysis of IPT Systems for Electric Vehicles Dynamic Battery Charging . . . 116**Giulia Di Capua¹, Luca De Guglielmo² and Nicola Femia²¹Department of Electrical and Information Eng., University of Cassino and Southern Lazio, Cassino, FR, Italy; ²Department of Information and Electrical Eng. and Applied Math., University of Salerno, Fisciano, SA, Italy**A7.3 Coil Geometry Modeling and Optimization for a Bidirectional Wireless Power Transfer System 120**

Simon Nigsch, Falk Kyburz and Kurt Schenk,

Institute for Energy Systems, Eastern Switzerland University OST, Buchs SG, Switzerland

A7.4 Impact of the Pad Geometry on System-Level Performance Indicators in WPT Systems for Electrical Vehicles 124Antonio Maffucci¹, Salvatore Ventre¹ and Alberto Delgado Exposito²¹Dep. of Electrical and Information Engineering, Univ. of Cassino and Southern Lazio, Cassino, Italy;²Centre of Industrial Electronics (CEI), Universidad Politécnica de Madrid, Madrid, Spain**A8 | Complex System Analysis II**

Chair: Jürgen Scheible, Reutlingen University, Germany

A8.1 A Probe Placement Method for Efficient Electromagnetic Attacks 128

Minmin Jiang and Vasilis Pavlidis, Advanced Processor Technologies group, Department of Computer Science, University of Manchester, Great Britain

A8.2 Dealing with hierarchical partitioning in bottom-up design methodologies 132F. Passos^{1,2}, Pablo Saraza-Canflanca¹, Rafael Castro Lopez¹, Elisenda Roca¹ and Francisco V. Fernandez¹¹Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Sevilla, Spain;²Instituto de Telecomunicações, Lisboa, Portugal**B1 | Analog Circuit and System Engineering**

Chair: Helmut Graeb, Technical University of Munich, Germany

B1.1 Modeling and Optimization of Supply Sensitivity for a Time-Domain Temperature Sensor 136

Jun Tan, IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany

- B1.2 Noise behavior in current mirror circuit based on CNTFET and MOS Devices..... 140**
 Roberto Marani¹ and Anna Perri²
¹National Research Council of Italy (CNR), Institute of Intelligent, Industrial Technologies and Systems for Advanced, Manufacturing (STIIMA), Bari, Italy; ²Department of Electrical and Information Engineering, Electronic Devices Laboratory, Polytechnic University of Bari, Bari, Italy
- B1.3 A g_m/I_D Sizing Method for High-speed Multi-stage Operational Amplifiers with Feedforward-only Compensation 144**
 Qixu Xie, Guoyong Shi and Yaoyao Ye, Dept of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai, China
- B1.4 Hybrid Capacitor-less LDO with Switched-Mode Dead-Zone Control..... 148**
 Nellie Laleni, Andreas Tsioungkos and Vasilis Pavlidis, Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, Greece

B2 | Behavioral Analysis

Chair: Georg Gläser, IMMS GmbH, Germany

- B2.1 Verilog-A model development of a DC–DC boost controller with autonomous optimization .. 152**
 Davide Severin¹, Giovanni Capodivacca¹, Bernard Blaise Tchodjie Tchamabe¹, Andi Buzo² and Cristian-Vasile Diaconu³
¹Infineon Technologies, Italy; ²Infineon Technologies, Germany; ³Infineon Technologies, Romania
- B2.2 Analog Circuit Abstraction to SystemC-AMS Secured by Affine Forms 156**
 Ahmad Tarraf and Lars Hedrich, Institute for Computer Science, Goethe University Frankfurt, Germany
- B2.3 Simulating the impact of Random Telegraph Noise on integrated circuits 160**
 Pablo Saraza-Canflanca¹, Eros Camacho-Ruiz¹, Rafael Castro-Lopez¹, Elisenda Roca¹, Javier Martin-Martinez², Rosana Rodriguez², Montserrat Nafria² and Francisco Fernandez¹
¹Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Sevilla, Spain; ²Electronic Engineering Department (REDEC) group, Universitat Autònoma de Barcelona (UAB) Barcelona, Spain

B3 | Simulation Methods

Chair: Günhan Dündar, Bogazici University, Turkey

- B3.1 Connecting Energy Storages from Tool Independent, Signal-flow Oriented FMUs 164**
 Meik Ehlert¹, Jan Michael¹, Christian Henke¹, Ansgar Trächtler², Matthias Kalla³, Bakr Bagaber³, Bernd Ponick³ and Axel Mertens³
¹Scientific Automation, Fraunhofer Institute for Mechatronic Systems, Design IEM, Paderborn, Germany; ²Heinz-Nixdorf-Institute, University of Paderborn, Paderborn, Germany; ³Institute for Drive Systems and Power Electronics, Leibniz Universität, Hannover
- B3.2 Adaptive Simulation with HDL Control Module for Frequency Converting Circuits 168**
 Zoltan Tibenszky, Martin Kreißig, Corrado Carta and Frank Ellinger, Technische Universität Dresden, Dresden, Germany
- B3.3 Step Size Determination Approach for Aging Simulations in Analog Ics..... 172**
 Engin Afacan, Department of Electronics Engineering, Gebze Technical University

B4 | Procedural Design Automation

Chair: Daniel Marolt, Reutlingen University, Germany

- B4.1 Schematic Generation of Programmable Analog Neural Networks for Signal Processing . . . 176**
 Florian Aul, Nikoletta Katsaouni, Lukas Krischker, Sascha Schmalhofer, Marcel H. Schulz and Lars Hedrich
¹Institute for Computer Science, Goethe University Frankfurt, Germany; ²Institute for Cardiovascular Regeneration, Goethe University Frankfurt, Germany
- B4.2 Generators, Templates, and Code Generation for Flexible Automation of Array-Style Layouts 180**
 Benjamin Prautsch¹, Reimund Wittmann², Uwe Eichler¹, Uwe Hatnik¹ and Jens Lienig³
¹Fraunhofer IIS/EAS, Institute for Integrated Circuits, Division Engineering of Adaptive Systems, Dresden, Germany; ²IMST GmbH, Kamp-Lintfort, Germany; ³Dresden University of Technology, Dresden, Germany
- B4.3 Improvement of Simulation-Based Analog Circuit Sizing using Design-Space Transformation 184**
 Matthias Schweikardt and Jürgen Scheible, Electronics & Drives, Reutlingen University, Reutlingen, Germany
- B4.4 Machine Learning Based Procedural Circuit Sizing and DC Operating Point Prediction . . . 188**
 Yannick Uhlmann¹, Michael Essich², Matthias Schweikardt¹, Jürgen Scheible¹ and Cristóbal Curio²
¹Electronics & Drives, Reutlingen University, Reutlingen, Germany; ²Cognitive Systems, Reutlingen University, Reutlingen, Germany

B5 | Optimization Methods

Chair: Francisco Fernandez, Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC and Universidad de Sevilla), Spain

- B5.1 Surrogate-Assisted Multi-objective Differential Evolution based on Gaussian Process for Analog Circuit Synthesis. 192**
 Sen Yin, Wenfei Hu, Ruitao Wang, Zhikai Wang, Jian Zhang and Yan Wang, Institute of Microelectronics, Tsinghua University, China
- B5.2 A fast Structural Synthesis Algorithm for Op-Amps based on Multi-Threading Strategies . . 196**
 Inga Abel, Clara Kowalsky and Helmut Graeb, Technical University of Munich, Munich, Germany
- B5.3 An Essay on the Next Generation of Performance-driven Analog/RF IC EDA Tools: The Role of Simulation-based Layout Optimization 200**
 Ricardo Martins¹, António Gusmão^{1,2}, António Canelas¹, Fábio Passos^{1,3}, Nuno Lourenço¹ and Nuno Horta^{1,2}
¹Instituto de Telecomunicações, Lisboa, Portugal; ²Instituto Superior Técnico, Universidade de Lisboa, Portugal; ³Dialog Semiconductors, Lisboa, Portugal

B6 | Complex System Analysis I

Chair: Jürgen Scheible, Reutlingen University, Germany

- B6.1 An Efficient Modeling Approach for Large Ring Oscillator Based Ising Machines 204**
 Markus Graber, Nico Angeli and Klaus Hofmann, Integrated Electronic Systems Lab, Technical University of Darmstadt, Darmstadt, Germany

- B6.2 The Merging Technique to Simulate Synchronization Mode of Coupled Oscillators 208**
Sergey Rusakov and Mark Gourary, IPPM, Russian Academy of Sciences, Moscow, Russia

B7 | Digital Circuit and System Engineering

Chair: Rafael Castro Lopez, Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Spain

- B7.1 RTL Implementation of MCMC-based Constraints Solver 212**
Moemen Ahmed¹, Youssef Ahmed¹, Younan Nagy¹, Manar Adbel-Rahman¹, Khaled Salah²,
M. Watheq El-Kharashi¹, Ayub Khan²
¹Department of Computer and Systems, Faculty of Engineering, Ain Shams University, Cairo, Egypt;
²Siemens Digital Industries Software, Fremont, USA
- B7.2 A study of SRAM PUFs reliability using the Static Noise Margin 216**
Eros Camacho-Ruiz, Pablo Saraza-Canflanca, Rafael Castro-Lopez, Elisenda Roca, Piedad Brox
and Francisco Fernandez, Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC and
Universidad de Sevilla), Sevilla, Spain
- B7.3 Design and Optimization of a Control Algorithm for a Digital Low-Dropout Regulator in
System-on-Chip Applications 220**
Benedikt Ohse¹ and Jun Tan²
¹Ernst-Abbe-Hochschule Jena, Jena, Germany; ²IMMS Institut für Mikroelektronik- und
Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany
- B7.4 A Differential Public PUF Design for Lightweight Authentication 224**
Shengyu Duan^{1,2} and Gaole Sai^{3,4}
¹School of Computer Engineering and Science, Shanghai University, China; ²State Key Laboratory
of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, China;
³Guangdong Provincial Key Lab of Robotics and Intelligent System, Shenzhen Institutes of Advanced
Technology, Chinese Academy of Sciences, China; ⁴CAS Key Laboratory of Human-Machine
Intelligence-Synergy Systems, Shenzhen Institutes of Advanced Technology, China

B8 | Device Modelling (2)

Chair: Nuno Lourenço, Instituto de Telecomunicações, Portugal

- B8.1 Organic Transistor Parameter Estimation and Accurate Modeling for Process Optimiza-
tion. 228**
Rosalba Liguori, Gian Domenico Licciardo and Luigi Di Benedetto, Department of Industrial
Engineering University of Salerno, Fisciano (SA), Italy
- B8.2 Bias Temperature Instability Characterization and Modelling for 0.18 um CMOS under
Extreme Thermal Stress Conditions 232**
Yen Tran^{1,2}, Toshihiro Nomura¹, Mohamed Salim Cherchali¹, Claire Tassin¹, Yann Deval² and
Cristell Maneux²
¹Etudes et Production Schlumberger, Clamart, France; ²Laboratoire IMS, Universite de Bordeaux,
Talence, France

PRIME 2021

C1 | Digital Circuits and Subsystems

Chair: Miguel Garcia-Bosque, University of Zaragoza, Spain

- C1.1 Run-Time Adaptive Hardware Accelerator for Convolutional Neural Networks 236**
 Cristian Sestito¹, Fanny Spagnolo¹, Pasquale Corsonello¹ and Stefania Perri²
¹Department of Informatics, Modeling, Electronics and System Engineering – University of Calabria, Italy; ²Department of Mechanical, Energy and Management Engineering – University of Calabria, Italy
- C1.2 Design and Analysis of a Leading One Detector-based Approximate Multiplier on FPGA . . . 240**
 Salvatore Scarfone¹, Fabio Frustaci¹ and Stefania Perri²
¹Department of Informatics, Modeling, Electronics and System Engineering – University of Calabria; ²Department of Mechanical, Energy and Management Engineering – University of Calabria
- C1.3 Extending a RISC-V core with an AES hardware accelerator to meet IOT constraints 244**
 Anthony Zgheib, Olivier Potin, Jean-Baptiste Rigaud and Jean-Max Dutertre, Mines Saint-Etienne, CEA-Tech, Centre CMP, Gardanne, France
- C1.4 Memristive Logic-In-Memory Implementations: A Comparison 248**
 Pietro Inglese, Elena Ioana Vatajelu and Giorgio Di Natale, TIMA Laboratory, France

C2 | Data Converters (1)

Chair: Alexander Meyer, RWTH Aachen University, Germany

- C2.1 A 12-bit 100 MHz SAR ADC in 110-nm CMOS for MAPSs 252**
 Silvia Tedesco, INFN of Turin, Italy
- C2.2 A Timing Skew Correction Technique in Time-Interleaved ADCs Based on a $\Delta\Sigma$ Digital-to-Time Converter 256**
 Gabriele Bè, Mario Mercandelli and Luca Bertulessi, Politecnico di Milano, Italy
- C2.3 A low-noise high-speed comparator for a 12-bit 200-MSps SAR ADC in a 28-nm CMOS process 260**
 Luca Ricci, Luca Bertulessi and Andrea Bonfanti, Politecnico di Milano, Italy

C3 | Data Converters (2)

Chair: Alexander Meyer, RWTH Aachen University, Germany

- C3.1 A 2GS/s 10-bit Time-Interleaved Capacitive DAC for Self-Interference-Cancellation Application 264**
 Mazyar Abedinkhan Eslami, Danilo Manstretta and Rinaldo Castello, University of Pavia, Italy
- C3.2 Implementation of a Low Power Decimation Filter in a 180nm HV-CMOS Technology for a Neural Recording Front-End 268**
 Markus Sporer, Nicolas Graber, Steffen Moll, Stefan Reich and Maurits Ortmanns, University of Ulm, Germany

C4 | Automotive

Chair: Michael Hanhart, RWTH Aachen University, Germany

- C4.1 Analog Baseband Filter and Variable-gain Amplifier for Automotive Radars in 22 nm FD-SOI CMOS** 272
 Andres Seidel¹, Songhui Li¹, Laszlo Szilagyi¹, Corrado Carta¹, Jens Wagner^{1,2} and Frank Ellinger^{1,2}
¹Chair for Circuit Design and Network Theory, Technische Universität Dresden, Germany;
²CeTi, Center for Tactile Internet, Technische Universität Dresden, Germany
- C4.2 A Highly Linear High-Voltage Compliant Current Output Stage for Arbitrary Waveform Generation** 276
 Felix Schwarze, Florian Protze, Frank Ellinger and Christian Matthus, Technische Universität Dresden, Germany
- C4.3 A RISC-V-based System on Chip for High-Speed Control in Safety-Critical 650 V GaN-Applications** 280
 Mike Richter¹, André Lüdecke¹, Yoon-Cue Lee¹, Alexander Stanitzki¹, Alexander Utz¹, Günter Grau², Holger Kappert¹ and Rainer Kokozinski¹
¹Fraunhofer Institute for Microelectronic Circuits and Systems (IMS), Duisburg, Germany;
²advICo microelectronics GmbH, Recklinghausen, Germany
- C4.4 An Approach to Online Wear Out Monitoring of PCB Interconnects in Safety-Critical Systems** 284
 Saeid Yazdani¹, Werner Wolz¹, Rainer Engelhardt², Christian Schott¹, Ulrich Heinkel¹ and Daniel Kriesten³
¹TU Chemnitz, Germany; ²Steinbeis GmbH, Chemnitz, Germany; ³Hochschule Mittweida, Germany

C5 | Sensing Circuits (1)

Chair: Markus Sporer, University of Ulm, Germany

- C5.1 Experimental Investigation of Dielectric Loss Induced Noise in Charge Detection Systems for Cosmic Dust** 288
 Sebastian Kelz, Markus Groezing and Manfred Berroth, Institut für Elektrische und Optische Nachrichtentechnik, University of Stuttgart, Germany
- C5.2 Generalized comparison of the accessible emission limits of flash- and scanning LiDAR-systems** 292
 Roman Burkard¹, Reinhard Viga¹, Jennifer Ruskowski² and Anton Grabmaier¹
¹University of Duisburg-Essen, Germany; ²Fraunhofer IMS, Duisburg, Germany
- C5.3 A Mixed-Precision Binary Neural Network Architecture for Touch Modality Classification** .. 296
 Hamoud Younes^{1,2}, Ali Ibrahim^{1,2}, Mostafa Rizk² and Maurizio Valle¹
¹University of Genova, Italy; ²Lebanese International University, Bekaa, Lebanon

C6 | Sensing Circuits (2)

Chair: Markus Sporer, University of Ulm, Germany

- C6.1 A CMOS SPAD pixel with an integrated mixed-signal rotatory TDC** 300
 Sergio Moreno, Victor Moro and Angel Dieguez, University of Barcelona, Spain

- C6.2 Germanium – InGaZnO heterostructured thin-film phototransistor with high IR photo-response** 304
Hichem Ferhati, Fayçal Djeflal and A Bendjerad, University of Batna, Algeria

C7 | Power Circuits and Harvesting

Chair: Sebastian Kelz, University of Stuttgart, Germany

- C7.1 Integrated Hysteretic Controlled Regulating Buck Converter with Capacitively Coupled Bootstrapping** 308
Francarl Galea, Owen Casha, Ivan Grech, Edward Gatt and Joseph Micallef, University of Malta
- C7.2 Single-Inductor Dual-Output Buck Converter with Charge Recycling** 312
Kemal Ozanoglu and Gunhan Dundar, Bogazici University, Istanbul, Turkey
- C7.3 Design of an integrated Maximum Power Point Boost Converter for PV Submodules** 316
Léon Weihs, Michael Hanhart, Leo Rolff, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany
- C7.4 Design of a High PSRR Multistage LDO with On-Chip Output Capacitor** 320
Jonas Zoche, Michael Hanhart, Jan Grobe, Léon Weihs, Leo Rolff, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany

C8 | Circuits for Clock Generation and Optimization

Chair: Jonas Meier, RWTH Aachen University, Germany

- C8.1 Skew and Jitter Performance in CMOS Clock Phase Splitter Circuits** 324
Lorenzo Scaletti, Angelo Parisi and Luca Bertulesi, Politecnico di Milano, Italy
- C8.2 Entropy Analysis of RO-based Physically Unclonable Functions** 328
Guillermo Díez-Senorans, Miguel Garcia-Bosque, Carlos Sanchez-Azqueta and Santiago Celma University of Zaragoza, Spain
- C8.3 On the Behavior of a Wide Set of Oscillators: PUFs or TRNGs?** 332
Miguel Garcia-Bosque, Abel Naya, Guillermo Díez-Señorans, Carlos Sánchez-Azqueta and Santiago Celma, University of Zaragoza, Spain
- C8.4 A 55 MHz Integrated Crystal Oscillator with Chirp Injection Using a 28-nm Technology** ... 336
Lantao Wang, Adrian Arnold, Jonas Meier, Markus Scholl, Ralf Wunderlich and Stefan Heinen RWTH Aachen University, Germany

D1 | RF Circuits and Systems (1)

Chair: Christopher Nardi, RWTH Aachen University, Germany

- D1.1 A low-power 26.56-GHz LC-based DCO for multi-gigabit communication systems** 340
Pablo Jiménez-Fernández¹, Óscar Guerra¹, Rocío Del Río¹, Alberto Rodríguez-Pérez² and Enrique Prefasi²
¹Instituto de Microelectrónica de Sevilla, Spain; ²KDPOF, Spain

- D1.2 A Wide-Tuning-Range 55 GHz CMOS VCO on 22 nm FD-SOI Technology 344**
Zoltán Tibenszky, Corrado Carta and Frank Ellinger, Chair of Circuit Design and Network Theory,
Technische Universität Dresden, Germany
- D1.3 A Fully Integrated 28 GHz Class-J Doherty Power Amplifier in 130 nm BiCMOS 348**
Simone Veni¹, Michele Caruso², David Seebacher², Andrea Neviani¹ and Andrea Bevilacqua¹
¹University of Padova, Italy; ²Infineon Technologies, Villach, Austria
- D1.4 A Scalable CPW Circuit Model in Advanced CMOS Technologies for mm-Wave
Frequencies. 352**
Carla Moran Guizan¹, Peter Baumgartner¹ and Stefan Heinen²
¹Intel Deutschland, Germany; ²RWTH Aachen University, Germany

D2 | Biomedical Circuits (1)

Chair: Catherine Dehollain, Ecole Polytechnique Federale de Lausanne, Switzerland

- D2.1 A Sub-1 μ A Low-Power Low-Noise Amplifier with Tunable Gain and Bandwidth for EMG
and EOG Biopotential Signals 356**
Rafael Vieira¹, Ricardo Martins¹, Nuno Horta¹, Nuno Lourenço¹ and Ricardo Póvoa^{1,2}
¹Instituto de Telecomunicações, Lisboa, Portugal; ²Escola Superior Náutica Infante D. Henrique,
Paço de Arcos, Portugal
- D2.2 Transistor Downscaling toward Ultra-Low-Power, sub-100 μ m² and sub-Hz Oscillators 360**
Gian Luca Barbruni¹, Chiara Bielli², Danilo Demarchi² and Sandro Carrara¹
¹Ecole Polytechnique Federale de Lausanne, Switzerland; ²Politecnico di Torino, Italy
- D2.3 Electronic solution to compensate the effects of the temperature and the humidity on the
measurements of a capacitive sensor dedicated to an injection insulin pen 364**
Sylvain Joly¹, Albrecht Lepple-Wienhues¹ and Catherine Dehollain²
¹Valtronic Technologies, Switzerland; ²Ecole Polytechnique Federale de Lausanne, Switzerland

D3 | Biomedical Circuits (2)

Chair: Catherine Dehollain, Ecole Polytechnique Federale de Lausanne, Switzerland

- D3.1 A scalable spike detection method for implantable high-density multielectrode array. 368**
Mattia Tambaro¹, Elia Arturo Vallicelli², Gerardo Saggese³, Andrea La Gala⁴, Marta Maschietto¹,
Alessandro Leparulo¹, Antonio Strollo³, Marcello De Matteis⁴, Andrea Baschiroto⁴ and Stefano
Vassanelli¹
¹University of Padova, Italy; ²INFN, Milan, Italy; ³University of Naples „Federico II“, Italy;
⁴University of Milano, Bicocca, Italy
- D3.2 Current-reuse Low-Power Single-Ended to Differential LNA for Medical Ultrasound
Imaging. 372**
Olivia Mirea, Carsten Wulff and Trond Ytterdal, NTNU: Norwegian University of Science and
Technology, Trondheim, Norwa

D4 | RF Circuits and Systems (2)

Chair: Lantao Wang, RWTH Aachen University, Germany

- D4.1 Low Power High Linearity 14-23 GHz SiGe HBT Downconversion Mixer 376**
Syed Sharfuddin Ahmed and Hermann Schumacher, University of Ulm, Germany
- D4.2 A Mixer-Embedded Low Noise Amplifier for Mixer-First Direct-Conversion Wake-Up Receivers. 380**
Christopher Nardi, Alexander Kronig, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany
- D4.3 Make Some Noise: Energy-Efficient 38 Gbit/s Wide-Range Fully-Configurable Linear Feedback Shift Register 384**
Christoph Wagner¹, Georg Gläser², Thomas Sasse¹, Gerald Kell³ and Giovanni Del Galdo^{1,4}
¹Technische Universität Ilmenau, Germany; ²IMMS GmbH, Ilmenau, Germany; ³Technische Hochschule Brandenburg, Germany; ⁴Fraunhofer IIS, Ilmenau, Germany
- D4.4 Every Clock Counts – 41 GHz Wide-Range Integer-N Clock Divider 388**
Christoph Wagner¹, Georg Gläser², Gerald Kell³ and Giovanni Del Galdo^{1,4}
¹Technische Universität Ilmenau, Germany; ²IMMS GmbH, Ilmenau, Germany;
³Technische Hochschule Brandenburg, Germany; ⁴Fraunhofer IIS, Ilmenau, Germany

D5 | Devices and Reliability

Chair: Stefan Heinen, RWTH Aachen University, Germany

- D5.1 Modeling Ni/ β -Ga₂O₃ SBD interface properties 392**
Madani Labeled¹, Nouredine Sengouga¹, Afak Meftah¹, Jun Hui Park², Sinsu Kyoung³, Hojoong Kim² and You Seung Rim²
¹Laboratory of Semiconducting and Metallic Materials, Biskra university; ²Department of Intelligent Mechatronics Engineering, and Convergence Engineering for Intelligent Drone; ³Research and Development, Powercubesemi Inc.
- D5.2 Performance assessment of a new low-cost RF sputtered Schottky diode based on a-Si/Ti structure 396**
Hichem Ferhati, Fayçal Djeflal, A Bendjerad and A Benhaya, University of Batna, Algeria
- D5.3 Digitally Programmable Potentiometer Multistage Architecture with Switch Independent Linearity 400**
Giorgiana Catalina Ilie^{1,2}, Cristian Tudoran², Otilia Neagoe², Gheorghe Pristavu¹ and Gheorghe Brezeanu¹
¹On Semiconductor, Romania; ²University “Politehnica” of Bucharest, Romania
- D5.4 Reliability Investigation of 0.18 μ m CMOS for OilField Applications. 404**
Yen Tran^{1,2}, Toshihiro Nomura¹, Mohamed Salim Cherchali¹, Claire Tassin¹, Yann Deval² and Cristell Maneux²
¹Etudes et Production Schlumberger, Clamart, France; ²Laboratoire IMS, Universite de Bordeaux, France

D6 | Analog Circuits and Qubit Interfaces

Chair: Lotte Geck, Forschungszentrum Jülich, Germany

D6.1 A Cryogenic High-Voltage Amplifier for Ion Traps	408
Michael Sieberer ¹ , Christoph Sandner ¹ and Peter Hadley ²	
¹ Infineon Technologies, Villach, Austria; ² Graz University of Technology, Austria	
D6.2 Cryogenic RF Transimpedance Amplifier in 22 nm SOI-CMOS for Control of a Qubit	412
Ricardo Heinen ^{1,2} , Dennis Nielinger ¹ , Christian Grewing ¹ , Ralf Wunderlich ² and Stefan Heinen ²	
¹ Forschungszentrum Jülich GmbH, Jülich, Germany; ² RWTH Aachen University, Germany	
D6.3 A First Order-Curvature Compensation 5ppm/°C Low-Voltage & High PSR 65nm-CMOS Bandgap Reference with one-point 4-bits Trimming Resistor	416
Edoardo Barteselli ¹ , Luca Sant ² , Richard Gaggi ² and Andrea Baschiroto ¹	
¹ University of Milano – Bicocca, Italy; ² Infineon Technologies, Villach, Austria	
D6.4 Resource Efficient Sub-V_T Level Shifter Circuit Design Using a Hybrid Topology in 28 nm	420
Saikat Chatterjee and Ulrich Rueckert, CITEC, Bielefeld University, Germany	