

## CONTENTS

INTRODUCTION.....	8
1 Scope.....	9
2 Normative references .....	9
3 Terms and definitions .....	9
General.....	14
1.1 Purpose.....	14
1.2 Version number.....	14
1.3 System structure and architecture .....	14
1.4 System information flow .....	15
1.5 Command types .....	15
1.6 Bus units.....	16
1.6.1 Transmitters and receivers in bus units.....	16
1.6.2 Control gear.....	16
1.6.3 Input device .....	16
1.6.4 Single master application controller .....	16
1.6.5 Multi-master application controller .....	17
1.6.6 Sharing an interface.....	17
1.7 Bus power supply and load calculations.....	18
1.7.1 Current demand coverage .....	18
1.7.2 Maximum signal current compliance .....	18
1.7.3 Simplified system calculation.....	18
1.8 Wiring.....	18
1.8.1 Wiring structure .....	18
1.8.2 Wiring specification .....	18
1.9 Insulation.....	19
1.10 Earthing of the bus.....	19
1.11 Power interruptions at bus units.....	19
1.11.1 Different levels of power interruptions.....	19
1.11.2 Short power interruptions of external power supply .....	19
1.11.3 External power cycle .....	20
1.11.4 Short interruptions of bus power supply .....	20
1.11.5 Bus power down .....	20
1.11.6 System start-up timing .....	20
Electrical specification .....	22
2.1 General.....	22
2.2 Marking of the interface.....	22
2.3 Capacitors between the interface and earth .....	22
2.4 Signal voltage rating .....	22
2.5 Signal current rating.....	23
2.6 Marking of bus powered bus unit .....	23
2.7 Signal rise time and fall time.....	23
Bus power supply .....	25
3.1 General.....	25
3.2 Marking of the bus power supply terminals.....	25
3.3 Capacitors between the interface and earth .....	25

3.4	Voltage rating .....	25
3.5	Current rating .....	25
3.5.1	General current rating .....	25
3.5.2	Single bus power supply current rating .....	26
3.5.3	Integrated bus power supply current rating .....	26
3.5.4	Dynamic behaviour of the bus power supply .....	26
3.6	Bus power supply timing requirements .....	27
3.6.1	Short power supply interruptions .....	27
3.6.2	Short circuit behaviour .....	28
Transmission protocol structure .....		28
4.1	General .....	28
4.2	Bit encoding .....	28
4.2.1	Start bit and data bit encoding .....	28
4.2.2	Stop condition encoding .....	29
4.3	Frame description .....	29
4.4	Frame types .....	29
4.4.1	16 bit forward frame .....	29
4.4.2	24 bit forward frame .....	29
4.4.3	Reserved forward frame .....	29
4.4.4	Backward frame .....	29
4.4.5	Proprietary forward frames .....	29
Timing .....		30
5.1	Transmitter timing .....	30
5.1.1	Transmitter bit timing .....	30
5.1.2	Transmitter frame sequence timing .....	31
5.2	Receiver timing .....	31
5.2.1	Receiver bit timing .....	31
5.2.2	Receiver bit timing violation .....	33
5.2.3	Receiver frame size violation .....	33
5.2.4	Receiver frame sequence timing .....	33
5.2.5	Reception of backward frames .....	34
5.3	Multi-master transmitter timing .....	34
5.3.1	Multi-master transmitter bit timing .....	34
5.3.2	Multi-master transmitter frame sequence timing .....	35
Method of operation .....		35
6.1	Collision avoidance, collision detection and collision recovery .....	35
6.1.1	General .....	35
6.1.2	Collision avoidance .....	36
6.1.3	Collision detection .....	36
6.1.4	Collision recovery .....	37
6.2	Transactions .....	39
6.3	Send-twice forward frames and send-twice commands .....	39
6.4	Command iteration .....	39
6.5	Usage of a shared interface .....	40
6.5.1	General .....	40
6.5.2	Backward frames .....	40
6.5.3	Forward frames .....	40

6.6	Use of multiple bus power supplies .....	40
6.7	Command execution .....	41
	Declaration of variables .....	41
	Definition of commands .....	41
	Test procedures .....	41
9.1	General notes on test .....	41
9.1.1	Abbreviations .....	41
9.1.2	Ambient temperature .....	41
9.1.3	External power supply voltage and frequency .....	42
9.1.4	Measurement requirements .....	42
9.1.5	Test signal generators and bus voltage sources .....	42
9.1.6	Deviation from documentation .....	42
9.1.7	Test setup .....	42
9.1.8	Notation .....	42
9.2	General interface tests .....	48
9.2.1	Label and literature check .....	48
9.2.2	Interface marking check .....	48
9.2.3	Bus powered bus unit marking check .....	49
9.2.4	Bus power supply marking check .....	51
9.2.5	Insulation test .....	53
9.2.6	Capacitor check .....	54
9.3	Bus power supply tests .....	54
9.3.1	Voltage rating test .....	54
9.3.2	Voltage rise time test .....	55
9.3.3	Current rating test .....	55
9.3.4	Dynamic behaviour test .....	57
9.3.5	Power-on open circuit test .....	59
9.3.6	Power-on timing test .....	60
9.3.7	Power supply short interruptions test .....	61
9.3.8	Power supply short circuit test .....	62
9.3.9	Power supply current consumption test .....	63
9.4	Control device tests .....	64
9.5	Control gear tests .....	64
	Annex A (informative) Background information for systems .....	65
A.1	Wiring information .....	65
A.2	System architectures .....	66
A.2.1	General .....	66
A.2.2	Single master architecture .....	66
A.2.3	Multi-master architecture with one application controller .....	67
A.2.4	Multi-master architecture with more than one application controller .....	68
A.2.5	Multi-master architecture with integrated input device .....	69
A.2.6	Multi-master architecture with integrated input device and power supply .....	70
A.3	Collision detection .....	71
A.4	Timing definition explanations .....	72
A.4.1	General .....	72
A.4.2	Receiver timing .....	72
A.4.3	Transmitter timing .....	72

A.4.4	Grey areas .....	73
A.5	Maximum current consumption calculation explanation .....	73
A.5.1	Single bus power supply .....	73
A.5.2	Multiple bus power supplies .....	74
A.5.3	Redundant bus power supplies.....	75
A.6	Communication layer overview .....	76
A.6.1	General .....	76
A.6.2	Physical layer .....	76
A.6.3	Data link layer .....	76
A.6.4	Network layer .....	76
A.6.5	Transport layer .....	77
A.6.6	Session layer.....	77
A.6.7	Presentation layer.....	77
A.6.8	Application layer .....	77
	Bibliography .....	78
	Annex ZA (normative) Normative references to international publications with their corresponding European publications.....	79
	Figure 1 – IEC 62386 graphical overview .....	8
	Figure 2 – System structure example .....	15
	Figure 3 – Communication between bus units (example).....	15
	Figure 4 – Example of a shared interface .....	17
	Figure 5 – Start up timing example.....	21
	Figure 6 – Maximum signal rise and fall time measurements.....	24
	Figure 7 – Minimum signal rise and fall time measurements.....	24
	Figure 8 – Bus power supply current behaviour .....	27
	Figure 9 – Bus power supply voltage behaviour .....	27
	Figure 10 – Frame example .....	28
	Figure 11 – Bi-phase encoded bits .....	29
	Figure 12 – Bit timing example.....	30
	Figure 13 – Settling time illustration .....	31
	Figure 14 – Receiver timing decision example .....	33
	Figure 15 – Collision detection timing decision example .....	37
	Figure 16 – Collision recovery example .....	38
	Figure 17 – Current rating test signal .....	56
	Figure 18 – Dynamic behaviour test setup.....	57
	Figure 19 – Dynamic behaviour test signal .....	58
	Figure A.1 – Single master architecture example .....	67
	Figure A.2 – Multi-master architecture example with one application controller.....	68
	Figure A.3 – Multi-master architecture example with two application controllers .....	69
	Figure A.4 – Multi-master architecture example with integrated input device .....	70
	Figure A.5 – Multi-master architecture example with integrate input device and bus power supply .....	71
	Figure A.6 – Collision detection timing diagram .....	72

Figure A.7 – Transmitter and receiver timing illustration.....	73
Figure A.8 – Bus power supply current values .....	74
Figure A.9 – Current demand coverage .....	74
Figure A.10 – Combination of 4 bus power supplies.....	75
Figure A.11 – Redundant bus power supplies .....	75
Table 1 – System components .....	14
Table 2 – Transmitters and receivers in bus units .....	16
Table 3 – Power-interruption timing of external power.....	19
Table 4 – Power-interruption timing of bus power .....	19
Table 5 – Short power interruptions.....	20
Table 6 – Start-up timing.....	21
Table 7 – System voltage levels .....	22
Table 8 – Receiver voltage levels.....	22
Table 9 – Transmitter voltage levels.....	23
Table 10 – Current rating .....	23
Table 11 – Signal rise and fall times.....	24
Table 12 – Bus power supply output voltage.....	25
Table 13 – Bus power supply current rating.....	26
Table 14 – Bus power supply dynamic behaviour.....	26
Table 15 – Short circuit timing behaviour.....	28
Table 16 – Transmitter bit timing .....	31
Table 17 – Transmitter settling time values.....	31
Table 18 – Receiver timing starting at the beginning of a logical bit.....	32
Table 19 – Receiver timing starting at an edge inside of a logical bit.....	32
Table 20 – Receiver settling time values .....	34
Table 21 – Multi-master transmitter bit timing .....	35
Table 22 – Multi-master transmitter settling time values.....	35
Table 23 – Checking a logical bit, starting at an edge at the beginning of the bit .....	36
Table 24 – Checking a logical bit, starting at an edge inside the bit.....	37
Table 25 – Collision recovery timing.....	38
Table 26 – Transmitter command iteration timing.....	40
Table 27 – Receiver command iteration timing.....	40
Table 28 – Function call keywords.....	43
Table 29 – Defined operators .....	46
Table A.1 – Maximum cable length.....	66
Table A.2 – OSI layer model of IEC 62386 .....	76